WHAT IS CLAIMED IS:

1. A method for reducing strapping devices in a computer system having at least one configurable device, the method comprising:

(a) providing a configuration value stored in a non-volatile memory;

(b) asserting a processor reset signal and a bus reset signal of a high-speed peripheral bus, wherein the high-speed peripheral bus is included in the computer system;

(c) fetching the configuration value from the non-volatile memory when an operation clock reaches its working voltage and frequency, wherein the high-speed peripheral bus works at the operation clock;

(d) repeating the step (c) until a most significant bit (MSB) of a fetched configuration value changes from a first state to a second state;

(e) asserting the configuration value fetched from the non-volatile memory to the at least one configurable device to configure the configurable device; and

(f) deasserting the processor reset signal, thereby the at least one configurable device is configured completely.

2. The method of claim 1, wherein the step (c) comprises:

deasserting the bus reset signal of the high-speed peripheral bus when the operation clock of the high-speed peripheral bus reaches working voltage and frequency; and

fetching the configuration value from the non-volatile memory.

3. The method of claim 1, wherein the step (e) comprises:

latching the fetched configuration value within a first bridge logic; and

asserting a strapping ready signal by the first bridge logic;

transporting the fetched configuration value from the first bridge logic to a second bridge logic; and

configuring the at least one configurable device in response to the fetched configuration value from the first bridge logic.

4. The method of claim 1, wherein the step (d) repeats the step (c) until the MSB of the fetched configuration value changes from a logic "1" to a logic "0".

5. The method of claim 3, further comprising:

latching run-time programmable configuration information when a run-time programmable configuration write signal is asserted.

6. The method of claim 1, wherein the step (a) comprises:

reserving a 64-bit memory space within a basic input/output system (BIOS) area;

programming the MSB bit of the configuration value into the second state to indicate an initialization strapping status of the computer system; and

storing the configuration value into the 64-bit memory space in the non-volatile memory.

7. An apparatus for reducing strapping devices in a computer system having at least one configurable device, comprising:

a peripheral bus;

a non-volatile memory, coupled to the peripheral bus, having a reserved space to store a configuration value for the at least one configurable device; and

a bridge logic, coupled to the peripheral bus, comprising:

a latch, responsive to a configuration enable signal, to assert the configuration value to configure the at least one configurable device; and

a multiplexer, having an output port coupled to the latch, to assert the configuration value stored in the non-volatile memory on the output port during power-up and reset states of the computer system, and to assert run-time programmable configuration information on the output port during other operational states, based on a state of a strapping ready signal.

8. The apparatus of claim 7, wherein the reserved space is defined as the non-volatile memory hexadecimal address range from FFFFFFD0 ~ FFFFFFD7 to accommodate the configuration value.

9. The apparatus of claim 7, wherein the configuration enable signal is asserted except when the strapping ready signal is asserted and a run-time programmable configuration write signal is deasserted.

10. The apparatus of claim 7, wherein the peripheral bus is an ISA bus.

11. The apparatus of claim 10, wherein the bridge logic is a PCI-to-ISA bus bridge.